DESIGNING SPACE COMPRESSOR FOR SYSTEM-ON-CHIP TEST

Satyendra N. Biswas[1] and Sunil R. Das[2, 3]

[1]Department of Electrical Engineering Technology, Georgia Southern University, Statesboro, GA 30460, USA
[2]School of Information Technology and Engineering, Faculty of Engineering, University of Ottawa, Ottawa, ON K1N 6N5, Canada
[3]Department of Computer and Information Science, College of Arts and Sciences, Troy University, Montgomery, AL 36103, USA

Introduction

AN enormous amount of complexity has been introduced to the test generation process of integrated circuits (ICs) due to very large-scale integration. With the unprecedented growth in the electronics industry, the integration densities besides system complexities continued to increase and hence, the need for better and more efficient methods of testing to assure reliable operations of chips, the mainstay of today's many sophisticated devices and products, was intensely felt [1–6].This complexity is primarily due to the reduction in the ratio of externally accessible nodes to internal inaccessible nodes in the circuit. **BIST** is a design methodology that has the capability of solving many of the problems otherwise encountered in testing digital systems. It combines the concepts of built-in test (BIT) and self-test (ST) in one, termed BIST. In BIST, a circuit module (chip, board or system) can test itself; in other words, the testing procedures (test generation, test application and response verification) are accomplished through built-in hardware. It allows different parts of a chip to be tested in parallel, thus reducing the required testing time and also eliminating the need for external test equipment. As the cost of testing is becoming the major bottleneck of the manufacturing expenditure of a new product, BIST tends to reduce manufacturing, test and maintenance costs and at the same time improves diagnosis. Several companies such as Motorola, AT&T, IBM and Intel have incorporated BIST in many of their products. As the cost of testing is becoming the single major component of the manufacturing expense of a new product, BIST thus tends to reduce the manufacturing and maintenance costs through improved diagnosis. BIST is widely used to test embedded regular structures that exhibit a high degree of periodicity such as memory arrays (SRAMs, ROMs, FIFOs and registers). This type of circuits does not require complex extra hardware for test generation and response compaction. A typical BIST architecture, as shown in Fig. 1, uses a test pattern generator (TPG) that sends its outputs to a circuit under test (CUT) and output streams from the CUT are fed into a test data analyzer. A fault is detected if the test sequence is different from the response of the fault-free circuit. The test data analyzer is comprised of a response compaction unit (RCU), storage for the fault-free responses of the CUT and a comparator.

This paper focuses primarily on the response compaction process of BIST techniques that basically formulate into realizing appropriate means of reducing the test-data volume coming from the CUT to a signature. The response compaction in BIST is carried out through a space compaction unit followed by time compaction. A major challenge in realizing efficient space compaction in BIST is the development of techniques that are simple, suitable for on-chip ST, require low area overhead and have little adverse impact on the CUT performance. With this perspective in view, this paper proposes a technique for implementing space-efficient BIST support hardware with applications specifically targeted towards embedded cores-based system-on-chip (SOC) [1], extending the well known concepts of conventional switching theory and of compatibility relation as employed in the minimization of incompletely specified sequential machines, utilizing graph theoretic concepts of finding all maximal complete subgraphs or cliques of undirected graphs in the design [6, 7], based on optimal generalized sequence mergeability, as developed and applied by the authors in earlier works for detectable single stuck-line faults of the CUT [6].

Algorithms

The developed aliasing-free space compaction approach is comprised of a set of algorithms. The first algorithm is for computing the set of incompatible pairs [6, 7] of response data outputs of the CUT for logic AND/NAND, OR/NOR and XOR/XNOR, while the second algorithm is designed for finding their maximal compatibility classes (MCCs) using the knowledge of incompatible pairs based on the graph theoretic approach. The final algorithm constructs the desired space compression networks utilizing the information of the generated MCCs. A brief summary of the different algorithms is furnished below.

- *Algorithm* $\mathcal{A}$–This algorithm computes all incompatible pairs of the CUT output lines (pairs that do not produce 100% fault coverage) for logic AND/NAND, OR/NOR and XOR/XNOR.
- *Algorithm* $\mathcal{B}$–This algorithm finds the MCCs from the set of incompatible pairs of the CUT outputs as obtained by *Algorithm* $\mathcal{A}$.
- *Algorithm* $\mathcal{C}$–This final algorithm employs the knowledge of MCCs as obtained through *Algorithm* $\mathcal{B}$ to construct zero-aliasing space compactors for the CUT.

In order to design the compactors, first we have to use *Algorithm* $\mathcal{A}$ to find all the incompatible pairs. Based on the information of the incompatible pairs, the MCCs are next generated by utilizing *Algorithm* $\mathcal{B}$, and finally, by employing *Algorithm* $\mathcal{C}$, a new compressor circuit is designed.

Experimental results

To demonstrate the feasibility of the proposed zero-aliasing space compaction technique, extensive simulations were conducted on different ISCAS 85 combinational and ISCAS

89 full-scan sequential benchmark circuits. As illustration, a three-stage zero-aliasing compaction network for c432 combinational benchmark circuit is given in Fig. 2. Figures 3 and 4 provide the compaction ratio and hardware overhead, respectively, for ISCAS 89 full-scan sequential and ISCAS 85 combinational benchmark circuits.

Conclusions

This paper reports on developing new zero-aliasing space compression approach of response data outputs in BIST, specifically targeted for application to digital embedded cores-based SOCs. The suggested technique makes use of some well accepted concepts of conventional switching theory and graph theory, together with the general idea of compatibility relation as used in the minimization of incomplete sequential machines, in the selection of specific gates for merger of arbitrary but optimal numbers of output bit streams of the CUT for the generation of aliasing-free space compression networks.

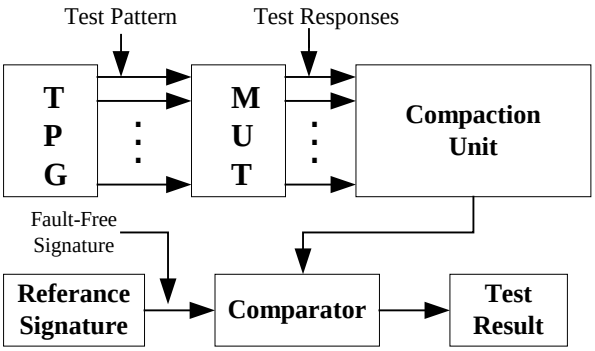

Fig. 1: A typical BIST environment.

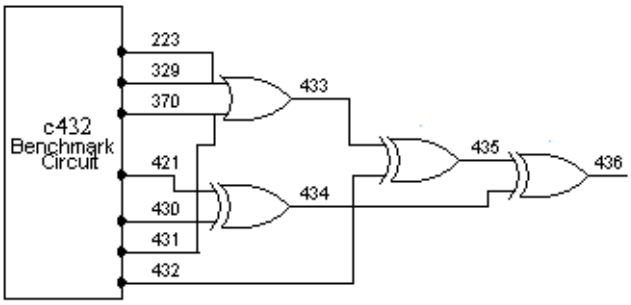

Fig. 2: Compactor circuit for c432 combinational benchmark circuit.

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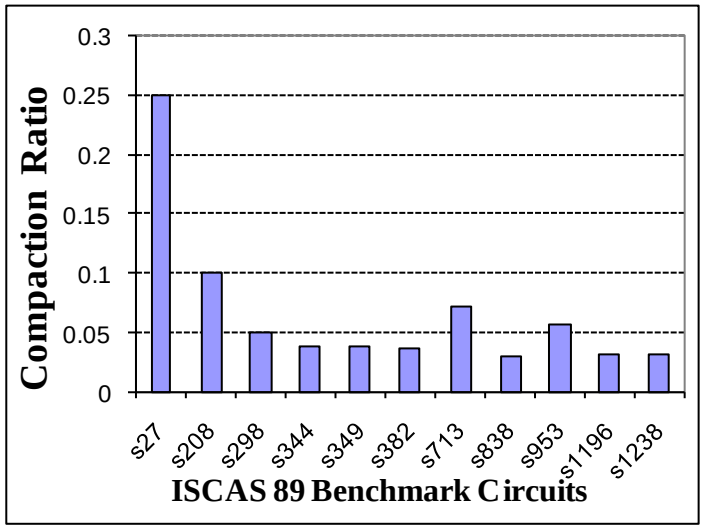

Fig. 3: Compaction ratio for ISCAS 89 full-scan sequential benchmark circuits.

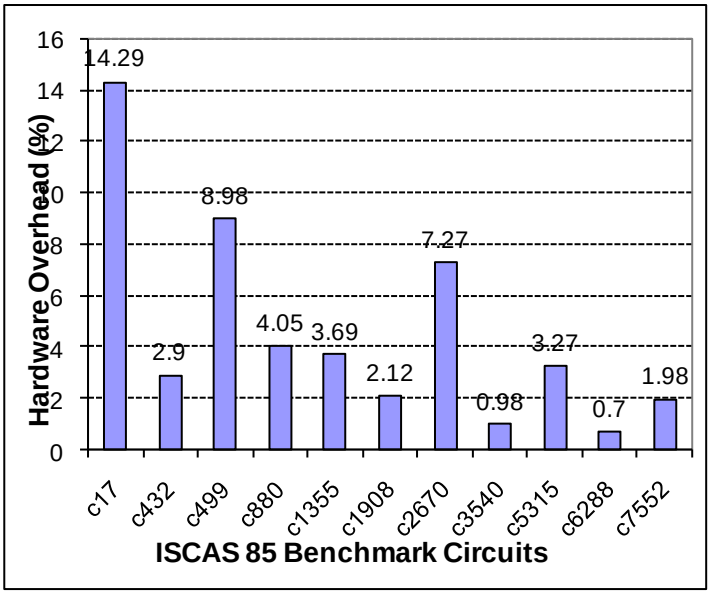

Fig. 4: Area overhead of compaction networks for ISCAS 85 combinational benchmark circuits.

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