Finite Element Analysis of 80Au/20Sn in an Interconnection Assembly

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Introduction

In electronic packaging applications, solder alloy is an important component [1]. Among solder alloys, eutectic Gold/Tin (AuSn) has wide applications [2]. In this study, finite element analysis was performed for fiducial-aligned placement process of an interconnection assembly. This assembly consists of a chip, a bonding pad, a solder strip, and a substrate. The material of solder strip will be modeled as thermal-elastic-plastic, and all other materials will be modeled as thermal elastic. The focus of the study will be on the behavior of the solder strip since it is one of the key components in the assembly.

Finite Element Model

The interconnection assembly consists of a silicon substrate which has a U-groove on its top surface. Inside the U-groove a Gold/Tin strip is placed. There is an indium phosphide chip on the top. The height of the strip is greater than the depth of the U-groove. As the chip is pressed down it deforms the Gold/Tin strip. A two-dimensional finite element model was created. Because of the symmetry, only half of the geometry is modeled. On the bottom of the substrate, it is assumed that there is no displacement in the *y*-direction.

The materials for chip (Inp, indium phosphide) and substrate (silicon) was modeled as linear elastic, and the eutectic Gold/Tin solder (80Au/20Sn) was modeled as thermal-elastic-plastic. These material properties are listed in Table 1, and shown in the figure 1.

Table 1. Material Property Data Summary

Material	E (GPa)	CTE (ppm/K)	ν	σ_s (Mpa)	Hardening Exponent
Inp	61.10	4.60	0.36		
Silicon	129.80	2.6	0.30		
Solder	58.313	16	0.406	217	0.03

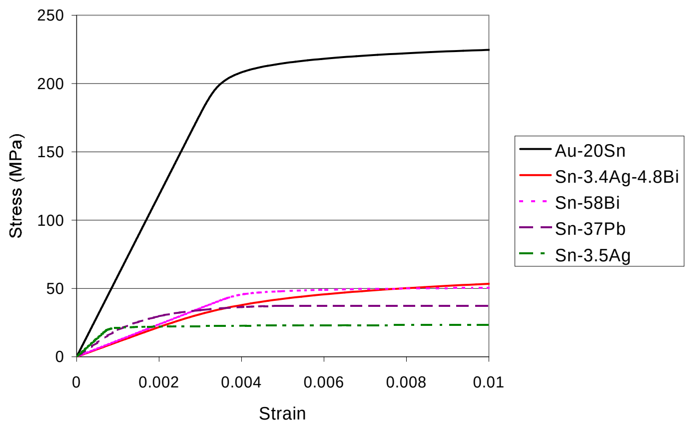

Fig 1. Elastic-Plastic Property of 80Au/20Sn

The process of fiducial-aligned placement is to push down the chip along with heat flux, which melts the solder, and make the solder in contact with the chip. So the loading conditions are simplified to two load steps. (1) Chip downward movement, $\Delta U_y = H_s - H_u$, where H_s and H_u are the height of solder strip and U-groove, respectively, and (2) Temperature increases, $\Delta T = 320^0 C - 25^0 C = 295^0 C$.

Finite Element Analysis Results

To ensure the reliability of the finite element analysis, convergence studies were conducted. From coarse to fine, there were 4 mesh systems

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that were created. For all these 4 mesh systems, a common reference point was chosen to output the stress and displacement components. The numerical results from mesh number 3 and number 4 were almost identical. So the final mesh was used in the analysis.

Deformed shape is shown in Figure 2. As expected, the solder has the maximum deformation.

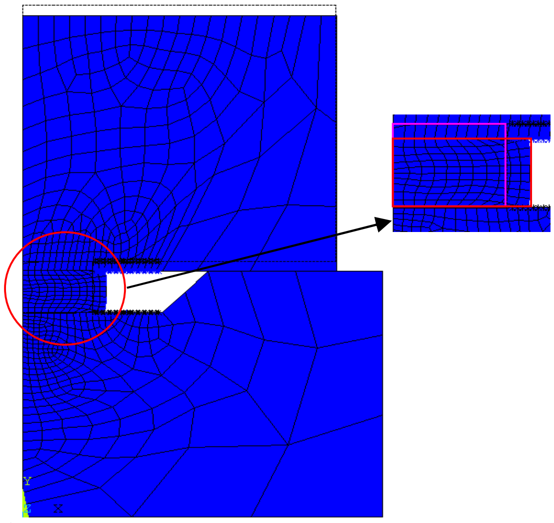

Fig 2. Deformed Shape

Figure 3 shows the contour plot of equivalent stress on the solder after the second load was applied. Figure 4 shows the contour plot of equivalent plastic strain. The maximum value of equivalent plastic strain is 3.056.

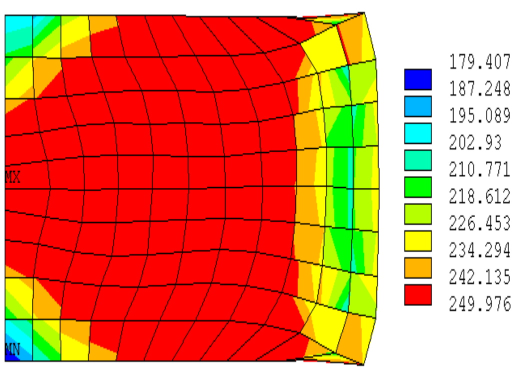

Fig 3. Contour Plot of Equivalent Stress

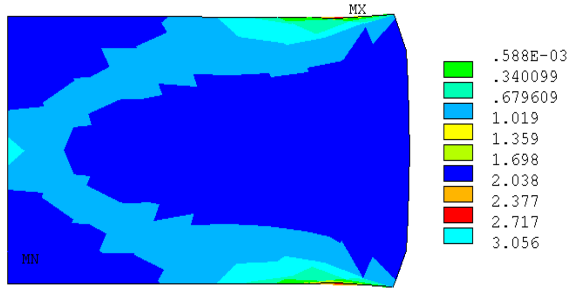

Fig 4. Contour Plot of Equivalent Plastic Strain

Summary

An elastic-plastic finite element analysis was conducted for fiducial-aligned placement process of an interconnection assembly. The process was simplified to two load steps. One is a displacement load, and the other a thermal load. When the chip is pushed down, the solder material is deformed. The area of solder material reduced in the *y*-direction roughly equals the new area of solder material gained in the *x*-direction. After the first load (vertical displacement) was applied, the maximum equivalent stress in the solder is 250 MPa, and the maximum equivalent plastic strain is 2.774. When the second load (thermal load) was applied, the distribution pattern of equivalent stress has some changes, but the magnitude of the maximum stress remains almost the same. The maximum equivalent plastic strain, however, has a 10% increase. The high stress/strain areas are near the two corners. These are the corners of solder and chip, and solder and substrate. Under the current load conditions, these two areas are the risky spots. Failure is most likely to occur in these areas if there is any failure in the structure.

References

1. Tummala, R.R., Rymaszewski, E.J., and Klopfenstein, A.G. "Microelectronics Packaging Handbook", Part I, 2nd Edition, Chapman & Hall, New York, (1997).
2. http://www.indium.com/gold

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