OPTIMIZATION IN FABRICATING 90NM NMOS UTILIZING TAGUCHI METHOD

Maizan Muhamad, Sunaily Lokman, Hanim Hussin

Faculty of Electrical Engineering,Universiti Teknologi MARA ,Selangor, Malaysia.

Introduction

In this paper, a 90 nm NMOS was designed and fabricated to study its electrical performance. ATHENA and ATLAS module of SILVACO software were the tools used in simulating the electrical performance of the NMOS transistor. Threshold voltage (VTH) value was the main parameter under investigation as it determines whether a transistor works or not. Other parameters were studied in this paper were the gate oxide thickness, Id-Vg and Id-Vd characteristics. From the simulation result, it was shown that gate oxide thickness, channel doping, V_{TH} adjust implant and the halo implantation contributed in determine the V_{TH} value and Id-Vg curve. From the simulation result, optimum solution is found in which V_{TH} and Tox values are 0.268011 and 0.25nm are achieved. This value is in line with International Technology Roadmap for Semiconductor (*ITRS*) value for 90nm.

Key-Words: 90nm NMOS, Silvaco, Taguchi

Variation factors

In order to find the optimum solution for fabricating the device, Taguchi method was utilized to find the sequence of dominance factors that determine the performance of 90nm NMOS. By utilizing Taguchi method, only selected sets of experiments need to be carried out, compared to many possible combinations. There are four factors that influence the threshold voltage values [3]. The purpose of this variation factor is to find which factor that more dominat in determine V_{TH} value. The variations values as follow:

- *Gate oxide thickness*
  i. Variation 1 – 0.00208um
  ii. Variation 2 – 0.00250um
  iii. Variation 3 – 0.00591um
- *V_{TH} adjust implant doping concentration*
  i. Variation 1 – Boron ($4.75x10^{9}$ atom cm^{-1})
  ii. Variation 2 – Boron ($9.5x10^{9}$ atom cm^{-1})
  iii. Variation 3 – Boron ($1.9x10^{10}$ atom cm^{-1})
- *Halo implant doping concentration*
  i. Variation 1 – Boron ($1.4x10^{13}$ atom cm^{-1})
  ii. Variation 2 – Boron ($2.8x10^{13}$ atom cm^{-1})
  iii. Variation 3 – Boron ($5.6x10^{13}$ atom cm^{-1})
- *Channel doping concentration*
  i. Variation 1 – Arsenic ($2.5x10^{15}$atom cm^{-1})
  ii. Variation 2 – Arsenic ($5x10^{15}$ atom cm^{-1})
  iii. Variation 3 – Arsenic ($1.0x10^{16}$ atom cm^{-1})

For all fourth factors above, variation 2 is taken from the simulation. Variation 1 is the variation 2 value divided by two while variation 3 is variation 2 value being doubled.

Results and Discussion

Figure 1 shows that Id versus Vg curve. Vd=0.2 is applied for this graph. When Vg < Vt, the current is zero but the current start increasing when Vg>Vt. With a small value of V_{DS} applied it is possible to examine the effect of an increase gate voltage.

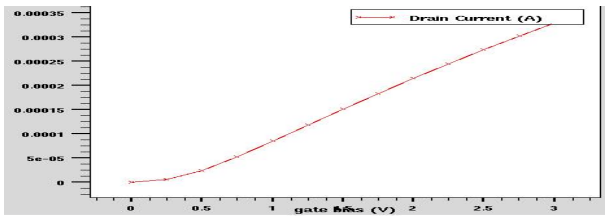

Figure 1: The Id versus Vg curve

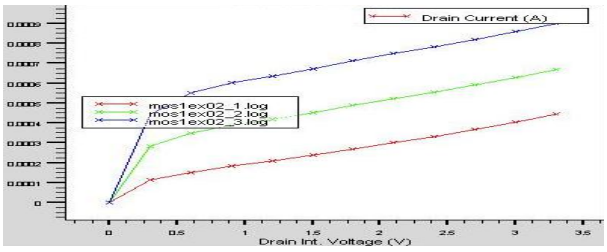

Figure 2: The Id versus Vd curve

Figure 2 show the curves of Id versus Vd for NMOS with voltage for red, green and blue line is 1.1V, 2.2V and 3.3V. The graph not saturated due to the punch through effect. Punch through causes a rapidly increasing current with increasing drain-source voltage. It is an extreme cause of channel length modulation where the depletion layers around the drain and source region merge into a single depletion region.

The optimum value of V_{TH} obatined from vary the factor is 0.2685. Halo implant contributes the most to the V_{TH} value.

Figure 3 shows effect of gate oxide thickness on threshold voltage. The oxidation time, temperature and pressure are the parameters that effect threshold voltage. Increase the gate oxide thickness, V_{TH} also increase [3].

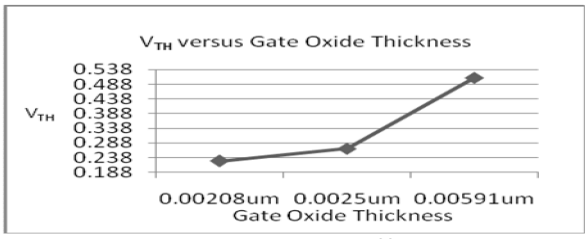

Figure 3: Treshold voltage at different gate oxide thickness

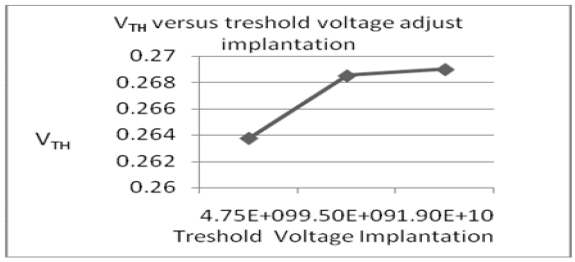

Figure 4: Variation of treshold voltage at different V_{TH} adjust implantation

Figure 4 shows the effect threshold voltage adjustment implantation to the threshold voltage. The threshold voltage adjust implantation alters the doping profile near the surface of silicon substrate [2]. A higher dosage of implant will lead to a higher V_{TH} value because the p-channel will be harder to invert for this NMOS transistor [1]. So, V_{TH} increase when V_{TH} adjust implantation doping increase.

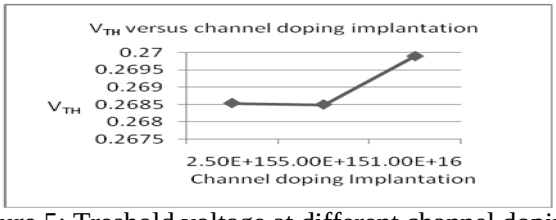

Figure 5: Treshold voltage at different channel doping

The figure 5 shows the threshold voltage increase when channel doping increase. When the channel doping increasing, the Fermi potential increases, also the channel depletion charge increasing, it takes more effort to deplete the whole channel. That cause the V_{TH} goes up when the chnnel doping increase [5].The doping of the channel is also depend on several parameters. The type of atom being implanted, the dosage and the energy are the parameters that effect the resulting doping concentration and depth[4].

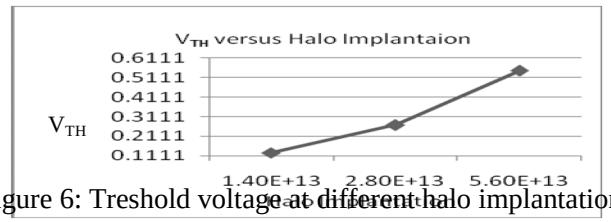

Figure 6: Treshold voltage at different halo implantation

Figure 6 show effect halo implantation to the treshold voltage. It can be seen that the value of treshold voltage increased as the dose of halo implantation increased. Besides that, threshold degradation can be controlled well since the halo implant reduces the charge sharing effects from source and drain[4]. Halo implantation is introduced to eliminate the effects of V_{TH} roll-out and short channel effect [6].

CONCLUSION

There are four factors that effect treshold voltage which is gate oxide thickness, V_{TH} adjust implantation, channel doping and halo implantation. From this simulation, the optimum V_{TH} value of 0.2685 is achieved. The value is in line with ITRS guideline for 90 nm NMOS. Halo implantation is contribute more in determine threshold voltage value. Besides that, the Id-Vd curve is not saturate due to punch through effect.

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