"Complementary Metal Oxide Semiconducor Compatibility of Carbon Nanotubes?"

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Abstract

It seems increasingly unlikely in the near future that carbon nanotubes (CNTs) will take over from silicon for use in the active devices such as transistors and diodes etc. in logic circuits. However their use in vias and interconnects in next generation integrated circuits is considered as being entirely feasible as is their use in transparent conducting contacts and in other plastic electronic applications. A major contribution to future electronics could be in tandem with Complementary Metal Oxide Semiconducor **(**CMOS) technology such as their use in sensors, thermal interface materials and solder joints. In this paper, the growth and characterisation of both single and multi wall CNTs is described and a realistic appraisal of the future of CNTs in CMOS will be provided.

Introduction

CMOS uses both N-type MOS and P-type MOS circuits. Since only one of the circuit types is on at any given time, CMOS chips require less power than chips using just one type of transistor. This makes them particularly attractive for use in battery-powered devices such as portable computers etc. As device dimensions continue to shrink, as faster and faster circuits are required, then the limits to conventional semiconductor devices is fast approaching. The ITRS road map and the roadmaps for several major companies indicate that carbon nanotube based transistors and logic circuits may have a major part to play in the future and indeed may eventually take over from silicon technology. There are still significant hurdles to overcome before this is achievable, if at all. However even if they are not able to take over from silicon for use in the active devices such as transistors and diodes etc. in logic circuits their use in vias and interconnects in next generation integrated circuits is considered as being entirely feasible as is their use in transparent conducting contacts. Another major contribution to future electronics could be in complementary applications to CMOS such as their use in sensors, thermal interface materials and solder joints.

CNTs are a unique form of carbon filament/fibre in which sheets of sp^2 bonded graphite with no surface broken bonds roll up to form tubes. Single Wall Carbon Nanotubes can exhibit either semiconducting or metallic like properties whereas Multiwall Carbon Nanotubes exhibit only non-semiconducting behaviour. Both types have been investigated for their use in electronics. To date there have been various reports of their use in transistors (1), diodes (2) and simple logic circuits (3), MEMS/NEMS (4), transparent ohmic contacts (5) and perhaps of more relevance to this presentation in vias and interconnects (6) and sensors (7). However there are still several problems to overcome before their potential in most of these applications can be realised.

Growth of CNTs

A number of methods have been developed for the growth of carbon nanotubes. Most of these can produce single wall CNTs or multiwall CNTs or a mixture of both. For many electronic applications, especially back-end applications i.e applications which involve growth of the CNTs onto the chip after the remainder of the chip has already been processed, it is imperative that the growth temperature be made as small as possible. This means that Chemical Vapour Deposition (CVD) methods are optimum. Over the past 10 or so years we have developed CVD deposition method to produce both SWCNT and MWCNTs (8). Most of these need temperatures in excess of 700 C. However even this relatively low deposition temperature is not compatible with growth on CMOS. More recently we have utilised remote plasma CVD to produce both MW and SWCNTs in-situ on Silicon on Insulator (SOI) substrates. A schematic of the growth system is shown in Figure 1. Here the process gas used was a mixture of $C_2H_2$and NH_3. The gases are decomposed by the graphitic heater at T = 800 C whilst the substrate is held at T=480-600 C or so. This enables us to grow CNTs (see fig 2) at temperatures compatible with CMOS technology.

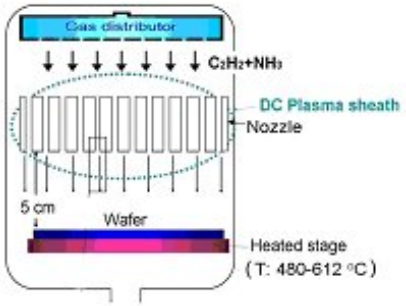

Figure 1 CVD System

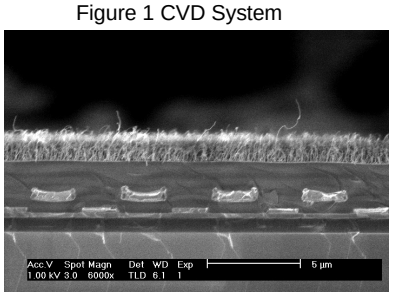

Figure 2 MWCNTs Grown on CMOS circuits

Applications

At present CNTs are better suited for applications which complement silicon rather than replace it. The remainder of the paper will thus describe some such applications. As device dimensions continue to decrease and as circuit complexity continues to increase the current densities/conductivity needed for connections between layers in 3-D structures (vias)- see figure 2 and the interconnecting lines between devices continue to increase. New conductors are required and CNTs with potential current density of 10^9A/cm2 are excellent candidates for both applications. It has been suggested that a nanotube density of at least 10^{13} cm^{-2} was needed in order to produce the required currents but recently Fujitsu have indicated that $5x10^{12}$ cm^{-2} would be acceptable [6]. Growing such dense arrays in vias of high aspect ratio is not so straightforward and much optimisation is still needed. Furthermore if CNTs are to be used as interconnects, methods of producing high density horizontal aligned CNTs is also needed. Work on this has also begun (9) but optimisation of the catalyst and growth process is still required**.** CNTs have also been suggested as a means to improv**e** the reliability of solder joints for high power devices by incorporation of the CNTs within the solder itself and their use with copper in thermal interface materials has also been touted. Finally a major activity in which CNTs or indeed alternative nanostructures can be used alongside silicon is in the area of smart gas sensors. Gas sensors are utilised in a variety of environments to detect e.g. CO_2, H_2, NO_X . Nanostructured materials are ideal candidates for gas sensing because of their high surface area to bulk. The aim of our work is to produce an integrated sensor/CMOS platform. The CMOS will be used to provide the interface circuitry, control for hot plates, biasing and signal filtering and amplification. The hot–plates are used to bring the sensing material to the optimum sensing temperature and also to provide a means of refreshing the sensing layers as described in (7). Room Temp response to NO_2 is shown below for our CNT sensors.

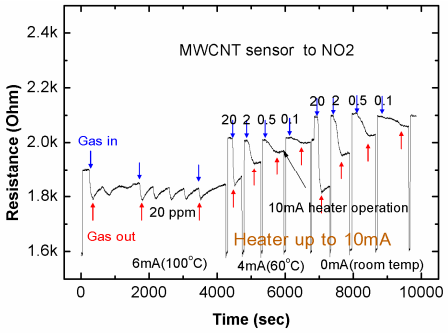

Figure 3 CNT Room Temp. response to NO_2.

Conclusions

The growth and some applications of CNTs in CMOS technology have been described. Their use in vias and interconnects is furthest advanced but their use in integrated sensors, thermal interface materials, in improved solder joints for power devices and also in transparent contacts also continues to be investigated.

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