TCAD MODELING STUDY OF THE STRESS MEMORIZATION PROCESS IN STRAINED SILICON DEVICES

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Introduction

Process induced uniaxial strain is an effective performance booster for the 90, 65 and 45nm node silicon devices because of increased asymmetric warpage of the energy bands, reduced carrier effective mass and increased density of states. The stress memorization technique (SMT) is one of several uniaxial strained silicon processes for n-channel devices [1]. It makes use of a temporary stress transfer dielectric capping layer which is tensile stressed and is etched away after an activation annealing step [1]. Although the SMT process has been implemented in manufacturing, its mechanism remains not well understood. Present explanations are based on the solid phase re-crystallization of amorphized polysilicon and lattice expansion [2] or plastic deformation effects in the polysilicon [3]. Due to the difficulty of measuring local strain in the nanoscale gate region, there is a lack of supporting experimental data. In this presentation, we use both computational and experimental results to obtain new insights into the SMT mechanism.

TCAD Modeling and Experiment

Sentaurus Process was used for the two dimensional (2D) stress simulations of a 50nm SMT nMOSFET with a polysilicon gate and a spacer made of $SiN_x/SiO_2/SiN_x$. SMT steps are performed after the self-aligned phosphorus source-drain implant. The process sequence consists of a Ge pre-amorphization implant (PAI) at 15keV and $3x10^{14}cm^{-2}$ followed by the deposition of 75nm of SiN_x with 1.8GPa tensile stress. Stress is transferred to the channel region by a rapid thermal anneal at 1050°C for 1s. The 2D spatial distributions of the stress tensor components, σ_{xx}, σ_{yy}, σ_{zz} during SMT are computed by numerically solving the quasi-static force equilibrium equations with Dirichlet boundary conditions. The dielectric layers (capping and spacer) are assumed to have Maxwell type viscoelastic stress-strain relations while polysilicon has anisotropic elastic properties. Calibrated values from the Sentaurus Process parameter database were used for all simulations.

In addition, a series of SMT nMOSFETs with gate lengths ranging from 60nm–1μm was fabricated using a similar SMT process. Device electrical characteristics were measured by a Keithley semiconductor characterization system (SCS-2400).

Results and Discussion

Fig. 1 shows the contour plots of σ_{xx} (along channel) after deposition of the +1.8GPa tensile SiN_x stressor. The top of the gate is under large compressive stress and in the y direction, the stress is similarly compressive. A plot for σ_{yy} was also obtained.

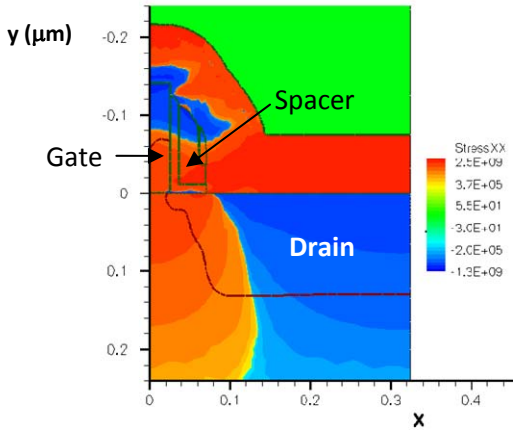

Fig. 1 Contour plot of σ_{xx} (Pa) after SiN_x deposition

After activation annealing, stress relaxation is found in the SiN_x stressor near the spacer where the tensile stress increased. This stress change is illustrated in fig. 2 as profiles of σ_{xx} before and after annealing extracted at y = -60nm (fig. 1). The relaxation of the SiN_x stressor due to viscoelasticity at 1050°C increases the tensile stress of the $SiN_x/SiO_2/SiN_x$ spacer. Due to the strong temperature dependence of the viscosity, relaxation is not possible after cooling and increased tensile stress is retained (or memorized) in the spacer. Hence, the tensile SiNx stressor can be etched away after the activation anneal. The final stress distribution consists of tensile σ_{xx} at the gate top and σ_{yy} (out of plane) in the spacer (fig. 3). The two pockets of compressive σ_{yy} at both channel ends are consistent with reference [1].

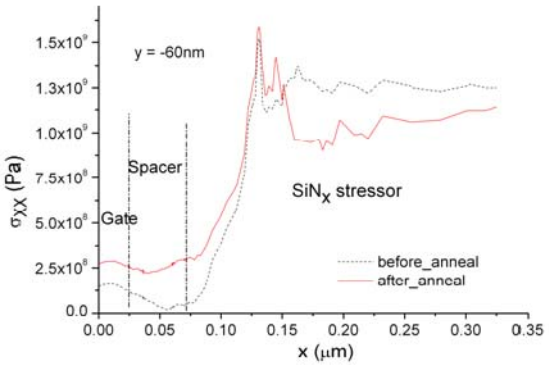

Fig. 2 Stress profile of σ_{xx} before and after rapid thermal anneal at 1050^0C for 1s

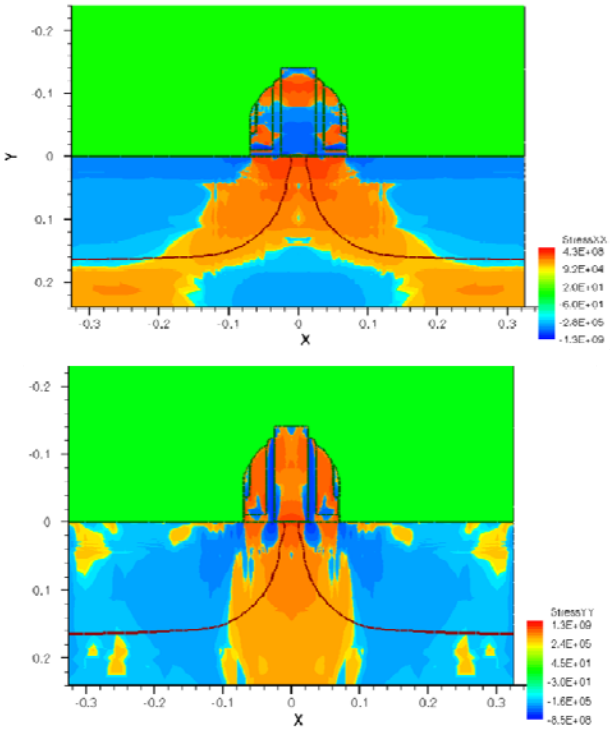

Fig. 3 Contour plot of (a) σ_{xx} (Pa) and (b) σ_{yy} (Pa) after SiN_x stressor etch. All lengths are in μm.

Fig. 4a-b shows σ_{xx} and σ_{yy} profile at 1nm below the silicon channel surface after SiN_x stressor etch. A non-uniform stress profile already exists before annealing. The profiles for 800^oC and 900^oC activation anneals are the same as no anneal and stress is enhanced only at higher anneal temperature.

According to simulation results (fig. 3), the mobility enhancement should depend on the gate length because of the non-uniform stress distribution in the channel. Fig. 5 shows the extracted effective mobility of the SMT device from I-V data decreases with gate length from 180nm to 1μm. The mobility degradation below 180nm is related to halo implant effect.

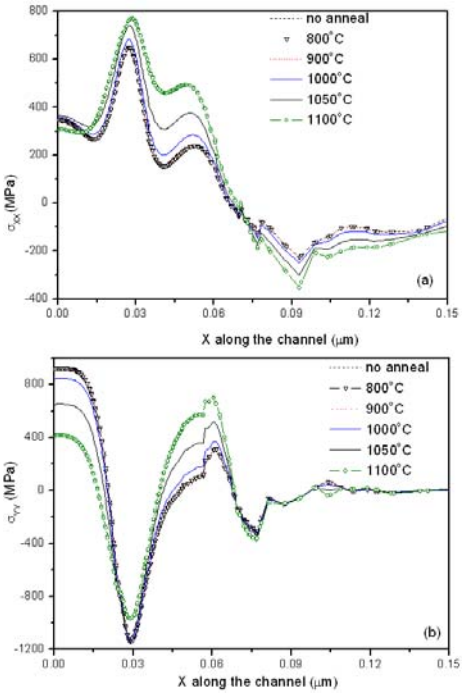

Fig. 4 Channel stress σ_{xx} (a) and σ_{yy} (b) at 1nm below Si surface for different anneal temperatures

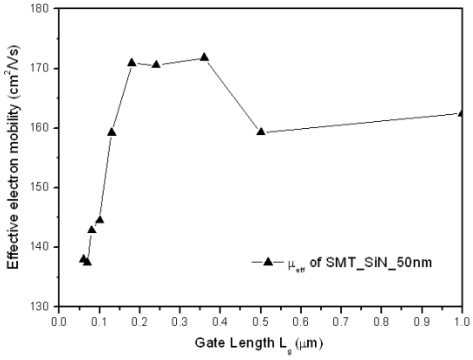

Fig. 5 Extracted effective electron mobility versus polysilicon gate length of SMT nMOSFETs.

Conclusion

In this study, both TCAD simulation and experiment show that the dielectric spacer play a more critical role in the SMT process than has hitherto been recognized.

References

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