SPACE COMPACTION IN VLSI USING CONDITIONAL FAULT DETECTION COMPATIBILITY

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Introduction

With unprecedented growth of the electronics industry, the integration densities and system complexities continued to increase, and hence, the need for superior and more effective methods of testing to assure reliable operation of chips, the mainstay of today's many sophisticated devices and products was intensely felt [1]–[7]. The very concept of testing generally has a broad applicability and finding highly efficient testing techniques that ensure correct system performance is of great practical significance. This complexity is primarily due to the reduction in the ratio of externally accessible nodes to internal inaccessible nodes in the circuit. Buit-in self-testing (BIST) is a design methodology that has the capability of solving many of the problems otherwise encountered in testing digital systems. It combines the concepts of built-in test (BIT) and self-test (ST) in one, termed BIST. In BIST, a circuit module (chip, board or system) can test itself; in other words, the testing procedures (test generation, test application and response verification) are accomplished through built-in hardware. It allows different parts of a chip to be tested in parallel, thus reducing the required testing time and also eliminating the need for external test equipment. As the cost of testing is becoming the major bottleneck of the manufacturing expenditure of a new product, BIST tends to reduce manufacturing, test and maintenance costs and at the same time improves diagnosis. Several companies such as Motorola, AT&T, IBM and Intel have incorporated BIST in many of their products. As the cost of testing is becoming the single major component of the manufacturing expense of a new product, BIST thus tends to reduce the manufacturing and maintenance costs through improved diagnosis. BIST is widely used to test embedded regular structures that exhibit a high degree of periodicity such as memory arrays (SRAMs, ROMs, FIFOs and registers). This type of circuits does not require complex extra hardware for test generation and response compaction. A typical BIST architecture uses a test pattern generator (TPG) that sends its outputs to a circuit under test (CUT) and output streams from the CUT are fed into a test data analyzer. A fault is detected if the test sequence is different from the response of the fault-free circuit. The test data analyzer is comprised of a response compaction unit (RCU), storage for the fault-free responses of the CUT and a comparator. This paper focuses primarily on the response compaction process of BIST techniques that basically formulate into realizing appropriate means of reducing the test data volume coming from the CUT to a signature. The response compaction in BIST is carried out through a space compaction unit followed by time compaction. This paper focuses on the problem of designing aliasing-free compaction networks for BIST of VLSI circuits using pseudorandom and compact test sets. A major challenge in realizing zero-aliasing space compaction in BIST is the development of techniques that are simple, suitable for on-chip ST, require low area overhead, and have little adverse impact on the CUT performance. With this perspective in focus, the subject paper proposes a new technique for implementing aliasing-free BIST support hardware with applications specifically targeted towards embedded cores-based system-on-chips (SOCs) [1]–[3], [7], extending some well known concept of conventional switching theory, *viz.* that of compatibility relation as employed in the minimization of incomplete sequential machines, based on pairwise sequence mergeability, for detectable single stuck-line faults of the CUT. The paper takes advantage of mathematically sound selection criteria of merger of a pair of output lines of the CUT by two-input XOR/XNOR logic for zero-aliasing, realizing maximal compaction in the design, as was apparent from extensive simulation experiments conducted on the International Symposium on Circuits and Systems (ISCAS) 85 combinational and ISCAS 89 full-scan sequential benchmark circuits using fault simulation programs ATALANTA and FSIM. In view of space constraints, only partial results on simulation using both ATALANTA and FSIM are provided here.

Algorithms Development

The developed aliasing-free space compaction approach is fundamentally comprised of two algorithms. The first stage of the proposed compression network is designed by carrying out **ALGORITHM** $\mathcal{A}$, while the second and subsequent stages of the compaction network are developed by using **ALGORITHM** $\mathcal{B}$, based on the concept of pairwise fault detection (FD) compatibility and *conditional* FD compatibility.

Simulation Experience and Conclusions

To demonstrate the feasibility of the proposed zero-aliasing space compression technique, extensive simulations were

conducted on different ISCAS 85 combinational and ISCAS 89 full-scan sequential benchmark circuits. In the design experimentation, we used ATALANTA (fault simulation program developed at the Virginia Polytechnic Institute and State University) as our test generation tool to generate the fault-free output sequences required to construct the space compactor circuits and to test the benchmark circuits using reduced test sets, accompanied with a random test session with FSIM fault simulation program that produces the necessary pseudorandom test vectors that detect most detectable single stuck-line faults for all the benchmark circuits. For each of the circuits, we computed the fault coverage before the compaction network, fault coverage with the compression circuit, number of applied test vectors, simulation CPU time, estimates of hardware overhead, and maximal compaction ratio. For designing the first stage of the compactor, **ALGORITHM** $\mathcal{A}$ is run first on the original CUT to generate an FD compatible pair and then *conditional* FD compatible pairs of output lines for merger with two-input XOR/XNOR logic. After generating the first stage of the compactor, a new CUT is formed, which is used for generating the second and subsequent stages of the compression network, by following **ALGORITHM** $\mathcal{B}$. The process of merger has to be continued until either a single output or a minimal number of outputs are eventually obtained. The data presented in Fig. 1 list each of the ISCAS 85 combinational benchmark circuits under test, number of test vectors applied to a circuit during testing, total number of faults injected into the circuit for each test, and fault coverage that was calculated as the baseline using FSIM. The data presented in Fig. 2 are for the same circuits using ATALANTA after the compressor was added. As the test simulation data demonstrate, the resulting area overhead of the compressors is pretty consistent with regard to the complexity of the CUT. With successful implementation of this methodology, it might be possible someday to automate the overall design process used for the compactors.

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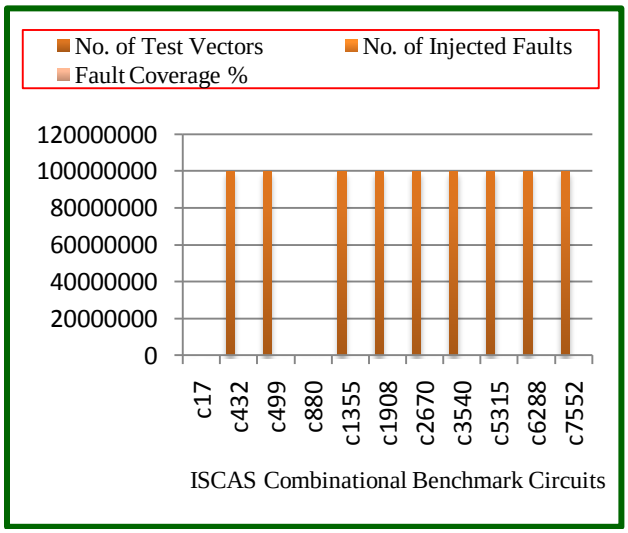

Fig.1. Fault coverage of ISCAS 85 combinational benchmark circuits using FSIM without space compactors.

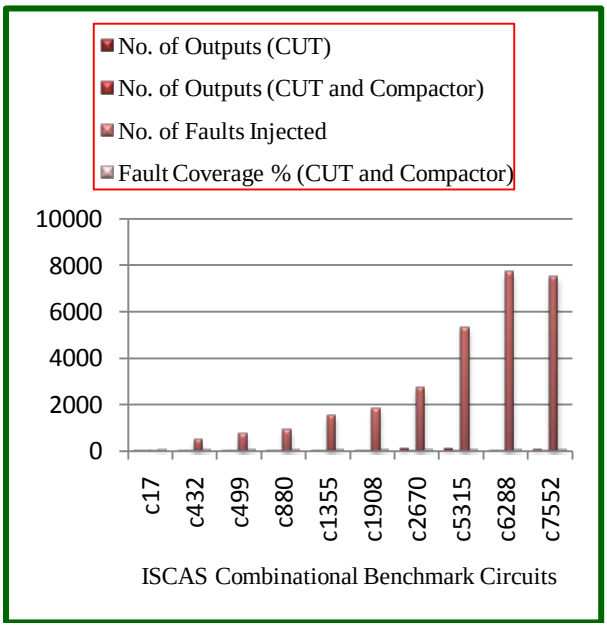

Fig. 2. Fault coverage of ISCAS 85 combinational benchmark circuits using ATALANTA with space compactor.

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