

Scaling Beyond Lithographic Limits – Polymer Self-Assembly Mediated Sub-20 nm FET devices

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Introduction

The relentless miniaturisation of electronic circuitry has spawned the ICT revolution that has impacted every aspect of modern life. This trend in scaling faces a number of challenges if the progress defined in International Roadmaps is to be delivered [1]. As well as fundamental physical limits such as interconnect related delay times and power issues there is the increasing cost of light sources for photolithography and implementing new mask/resist technologies. Scaling beyond the 32 nm node will require novel light sources as well as new mask and resist materials [2]. Device dimensions around 10 nm may demand implementation of ‘bottom-up’ substrate patterning methods using self-organisation or self-assembly of components rather than conventional top-down lithographies [3]. However, substrate patterning via chemical assembly is the basis of the ‘grand challenge’ of positioning since the reproducibility, placement accuracy and defect densities within the pattern have very exacting requirements. In this paper recent data on how self-organising (this is the more correct description since the systems show well resolved order-disorder transitions) block polymer (BCP) systems can be used to create nanocircuitry elements is discussed.

Experimental

Film Preparation: The principal BCP used was polystyrene-*b*-polymethylmethacrylate (PS-*b*-PMMA) with a polystyrene fractional mass content of 0.5 and a M_n value of 37 kg/mol was purchased from Polymersource Inc. of Quebec (Canada) and used as received. Other polymers used were PS-*b*-PFS, PS-*b*-PEO and PS-*b*-PI-*b*-PS (PFS = polyferrocenyldimethylsilane, PEO = polyethylene oxide and PI = polyisoprene). Full details on the polymers used are given elsewhere [4]. For PS-*b*-PMMA, 1 wt.% BCP in toluene solutions were spin coated on a Speciality Coating Systems G3P-8 spin-coater at 3000 rpm onto substrates. Simultaneous microphase separation and dewetting was achieved by placing vacuum heating for 24 hour at 180 °C. Substrates could be pre-treated by grafting of a polystyrene-polymethylacrylate (PS-*r*-PMMA) random copolymer brush (polystyrene content of 58%) by annealing a film at 160 °C for 48 hour under vacuum. Excess brush was stripped from the substrate by washing in toluene.

Thin film and nanostructure characterisation: SEM images were obtained using an Hitachi S4800 and FEI

Strata dual-beam 235 microscopes operating at 2-5 kV. In order to minimize charging effects, samples were coated with a thin layer of Pt by thermal evaporation methods. FIB cross-sectional samples were prepared using a FEI strata dual-beam 235 system.

Substrates: Substrates used were 8” silicon-on-insulator (SOI) samples (Soitec – France). The upper surface silicon was 70 nm thick and this was thinned back by oxidation and subsequent stripping to 30 nm.

Pattern transfer: Briefly, BCP was spincoated onto an SOI substrate to produce a nanopattern by microphase separation of the blocks (lamellar structure as shown) (A). An etch is then used to selectively remove one block (PMMA) so that a patterned resist layer (PS) is formed. Exposed silicon can then be removed by a silicon selective etch to leave a nanopatterned silicon surface (with some PS at the upper surface of the silicon structures). The method of pattern transfer is illustrated in figure 1. The removal of the PMMA was performed by dry etching with an Oxford plasmatech 100 using oxygen/tri-fluoromethane (O_2/CHF_3) mixture. Loss of PS was negligible due to etch selectivity. Silicon was etched via sequential CF_4/H_2 and SF_6/C_4F_8 etches on a STS (AGE) ICP instrument.

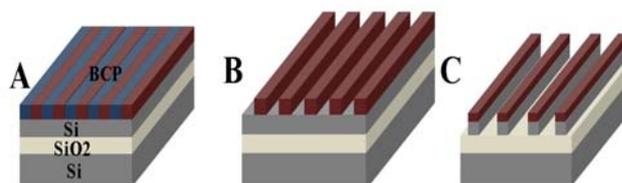


Fig. 1: Simple representation of the pattern transfer methodology.

Results and Discussion

The most challenging aspects of using self-organisation for nanodevices fabrication are probably associated with periodicity and positioning. Conventional lithography achieves the required placement accuracy within the pattern over 12” substrates [1]. Such accuracy in BCP systems can only be achieved by means of ‘directing’ the structure because films on simple substrates have limited periodicity and demonstrate ‘finger-print’ patterns (figure 2). Structural alignment is achieved by two principal methods, chemical [5] and graphoepitaxial patterning [6]. Chemical patterning uses x-rays, UV light or e-beams to pre-pattern a responsive surface to produce a pre-pattern that has differing chemical functionality and directs the

self-organisation of the BCP. In graphoepitaxy, a topographically patterned substrate also acts so as to align the structure in directions defined by the lithography. Typical graphoepitaxial (here, we use lithographically defined rectangular cross-section channels of around 60 nm depth) BCP nanopatterns for BCPS adapting a hexagonal arrangement of cylinders of one block in a matrix of the other are shown in figure 3. In the figure, the orientation of structure is determined by control of the surface chemistry through application of a brush layer.

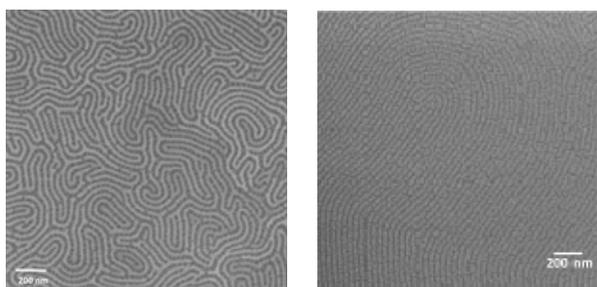


Figure 2: Striped lamellar PS-*b*-PMMA (left) and (right) hexagonal PS-*b*-PEO (42–11.5 kg mol⁻¹ block molecular weights) films on simple silicon substrates.

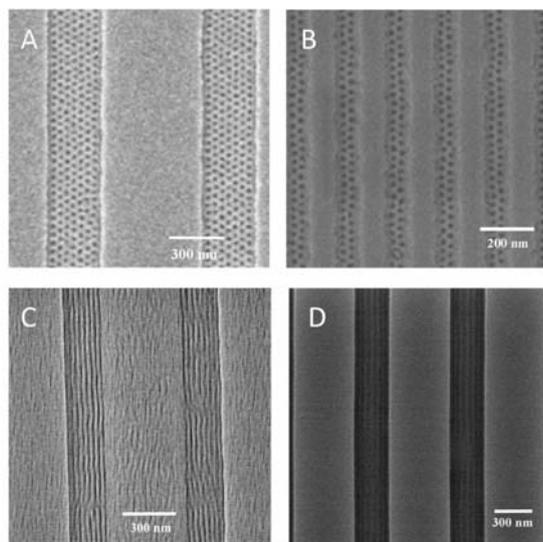


Figure 3: Hexagonally structured BCPs. Cylinders vertical (A,B – brushes present to produce a surface neutral to both blocks) and horizontal to surface (C,D). A,C=PS-*b*-PMMA, B=PS-*b*-PEO and D=PS-*b*-PFS

As above, the biggest challenge towards the use of these nanopatterns into real devices for circuit development is generating highly regular periodic structures over large surface areas and these nanopatterns must be effectively defect free. In graphoepitaxy, this is only possible through the control of chemistries at the base of the channel, the sidewalls and the mesas [2].

Finally, these polymeric patterns have to be converted into inorganic (e.g. silicon semiconductor wires) structures for fabrication of field effect transistors (FETs)

by pattern transfer as described in figure 1. All of the images shown in figure 2 and 3 are secondary electron microscopy images following a dry oxygen etch to remove the more reactive block (i.e. PMMA, PEO, PFS etc.) to leave the PS component (to act as a resist) and exposed silicon (oxide). On an SOI substrate, a suitable selective silicon etch followed by polymer strip (to remove the protective PS) will then leave patterned silicon surface (as a series of silicon nanowires for striped polymer nanopatterns). Typical results are shown in figure 4. This shows that parallel silicon nanowires (12–14 nm diameter) can be formed by this methodology and that wires retain the crystallinity of the SOI layer. Electrical characterisation confirms the wires are electrically similar to bulk Si. These results show that BCP lithography of this type may provide means to extend the development of Si-FETs towards their ultimate performance.

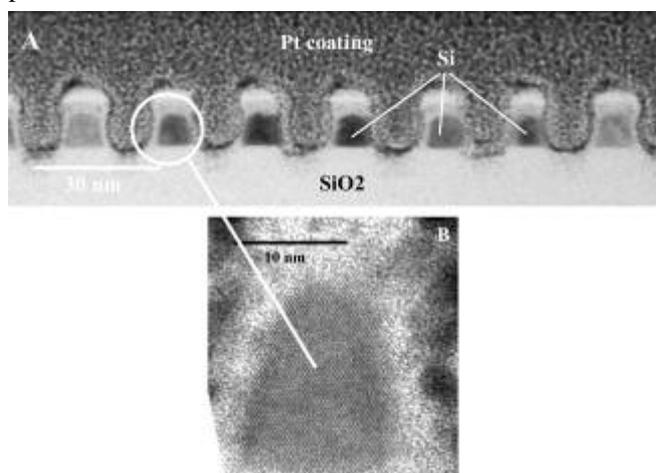


Figure 4. X-section of Si nanowires formed by BCP pattern transfer to the Si layer of an SOI substrate

Acknowledgements

The authors wish to acknowledge the SFI CRANN CSET grant for support for this programme. The Tyndall National Institute are thanked for processing support

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