FABRICATION OF 2D SILICON NANO-MOLD BASED ON SIDEWALL PATTERN TECHNIQUE

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Introduction

Some basic phenomena are unique to nanochannels, such as ion transport [1], concentration polarization [2], capillarity, and voltage responsive structures [3]. Nanochannels have the potential to be used in various applications in chemistry, biology and physics. In this research, a nano-mold with 200nm wide, 200nm high and 4.3mm long used for nanochannels have been fabricated by top-down processing method.

A sidewall pattern technique is the patterning technique proposed to break the resolution limit of the conventional ultraviolet lithography equipment. Sidewall pattern is a technique which can achieve narrow width of a pattern structure by thin-film coating on the sidewalls of supporting structures and selectively etching away the supporting structures. The nanopattern structures fabricated by using the sidewall pattern technique were also reported [4, 5].

Generally, the process of obtaining a sidewall pattern is performed by the deep reactive ion etching (DRIE) equipment. The sputter etching of a gold layer is performed by argon gas, and, since this is a physical process, it does not form any volatile compounds. The sputtered material can redeposit anywhere inside the sputtering chamber causing its contamination, and thus, influencing the following processes with other materials inside the chamber of DRIE equipment. Consequently, the thin film deposition system (Kurt J. Lesker, LAB18) was chosen to carry out a selective removal of the horizontal gold layer.

Experimental

Fig.1 shows schematic diagram of the 2D silicon nano-mold fabrication by using a sidewall pattern method. The process is described as follows:

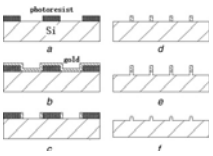


Figure 1. Schematic of the sidewall pattern fabrication procedures.
a. photoresist supporter fabrication; b. gold sputtering; c. sputter etching; d. photoresist supporter removing; e. DRIE; f. finished 2D silicon nano-mold.

In the step a, the silicon wafer is cleaned and the photolithography is performed; in step b, the 200nm gold layer is sputtered employing a thin film deposition system.

In the step c, argon sputter etching is performed in the thin film deposition system. The shutter plate and the shell of the chamber are used as the positive electrode and the wafer holder plate as the negative electrode. The distance between the two plates is set to be 36 mm.

The wafer holder plate can be static or rotated and the shutter plate can be opened or closed.

Four sets of experiments has been done and the sputter etching parameters are: chamber vacuum in the range of 3.0E-7 to 3.5E-7 torr before the sputter etching, chamber pressure in the range of 7.25E-3 torr to 7.35E-3 torr, 100W RF power, argon gas flow between 54.5sccm and 55sccm, 10 mtorr argon pressure during the process of sputter etching. The other conditions of the sputter etching are listed in Table 1.

Table1 Conditions of the sputter etching

Sample	Wafer holder plate	Shutter plate	Plasma glow
A11	20 rpm rotary	closed	instability
A12	20 rpm rotary	open	instability
A13	static	closed	stability
A14	static	open	stability

Results and Discussion

The plasma glow in the chamber was not stable when the wafer holder plate was rotated, indicated by its non-uniform appearance. The one possible reason is that the rotating cathode gives rise to a gas flow disturbing for the plasma glow. The other reason is a low argon gas flow which is insufficient to generate the plasma. The argon flow could be increased to overcome this effect, but for the price of a diversed argon ion directionality because of the higher chamber pressure.

The plasma glow in the chamber was stable only when the wafer holder plate was static. The shell of the chamber was used as the anode, the wafer holder plate as the cathode while the shutter plate was open. At this case most of the argon ions would not vertically bombard the wafer and therefore the gold layer was not selectively removed.

To improve the argon ion directionality, the wafer holder plate was kept static and the shutter plate closed for the process of gold sputter etching. Fig. 2 shows that the horizontal gold layer is removed and the vertical side wall gold layer is left.

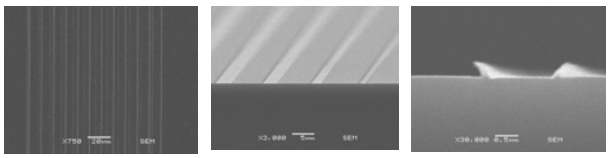


Figure 2. The scanning electron microscope(SEM) photographs of the gold sidewalls pattern.

The 2D silicon nano-molds with different line width were fabricated using the gold sidewall patterns and their widths were controlled by the sputter etching time. The nano-mold widths are 203nm, 114nm and 80nm from left to right respectively, as shown in Fig. 3.

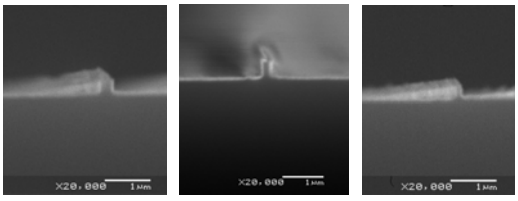
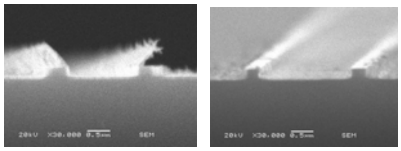


Figure 3. SEM views of the nano-molds with gold sidewalls in different widths.

The Fig. 4 shows (a) the shape of the gold sidewalls on the top of silicon after the deep reactive ion etching process (ALCATEL AMS100SE ICP) and (b) Silicon nano-molds with 200nm wide and 200nm high after the gold sidewall removal process.



(a) (b)

Figure 4. SEM views of the gold patterns on the top of Silicon (a) and nano-molds (b).

Conclusion

A 2D silicon nano-mold fabrication process with the side wall process over the full wafer size is presented. Nanoscale gold line patterns can be fabricated accurately, uniformly, and with a good reproducibility over the full wafer by using the physical sputter etching process without nanolithography. The width, depth, and length of the nano-mold can be precisely controlled by the sputter etching process and DRIE process. The reported nanochannel fabrication technique can be applied in the areas of the chemistry, biology and physics.

References

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