Synthesis and characterization of GaAs nanowires on amorphous substrates

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Abstract

Solid-source chemical vapor deposition method is developed for the synthesis of crystalline GaAs NWs with high growth yield using Ni thin film as catalysts on amorphous SiO_2/Si substrates. The NW growth parameters are optimized at the source temperature of 900 ^oC, substrate temperature of 600 ^oC and H2 flow rate of 100 sccm for 30 min. The obtained NWs have a narrow distribution of diameters (21.0 ± 4.0 nm), with the length exceeding 10 μm. The NWs are grown along different crystallographic directions with low defect densities observed.

1. Introduction

GaAs nanowires (NWs) are promising building blocks for nano-electronics, nano-photonics, photovoltaics, etc, due to the direct bandgap and high electron mobility [1, 2, 3]. To synthesize high quality GaAs NWs, MBE and MOCVD methods are commonly adopted following the well-known vapor-liquid-solid (VLS) and/or vapor-solid-solid (VSS) mechanism [1]. However, crystalline GaAs wafers are usually taken as the starting substrates for the epitaxial growth of GaAs NWs, which may limit the vast preparation and subsequent device integration. Thus there is an urgent need to explore crystalline GaAs NWs with high growth yield for technological applications.

2. Results and Discussion

2.1. Growth temperature optimization

In this study, GaAs NWs were synthesized by an enhanced solid-source CVD method, where GaAs powder was used as the precursor source and Ni thin film was used as the catalysts. Based on the VLS/VSS growth mechanism, the substrate temperature is one of the critical parameters to affect the NW synthesis and the substrate temperature was varied in a range between 560 ^oC and 640 ^oC with the source temperature kept at 900 ^oC to provide Ga and As (probably in the As_2 vapor form) in this case. During the growth, the hydrogen flow rate was maintained at 200 sccm and growth time was set for 60 mins. Figure 1(a) (b) and (c) show the SEM images of GaAs NWs grown at 560, 600 and 640 ^oC, respectively, where the NW density is found much higher grown at 600 ^oC even though with surface coatings. At the low substrate temperatures, Ni NCs, formed in annealing process, are far from the equilibrium liquid phase and only a small amount of NCs can form Ni-Ga alloy effectively, due to the melting point lowering effect of nanomaterials [4], to give low density of NWs. On the other hand, at high temperatures, as the congruent evaporation temperature of GaAs is found to be ~ 630 ^oC, As_2 has a much higher vapor pressure so that the decomposition of grown GaAs NWs is induced. Notably, the solid solubility of Ga in Ni NCs also get increased at such higher temperatures and this would further reduce the supersaturation to lower the NW growth yield [5]; therefore, the optimal substrate temperature was found at ~ 600 ^oC.

Moreover, the source temperature was explored between 850 and 900 ^oC, with typical results at 850, 875 and 900 ^oC illustrated in Figure 1 (d), (b) and (e), respectively. At lower source temperatures, there are inefficient precursors delivered for the NW growth, while at higher temperatures, more than sufficient precursors are evaporated to induce the significant tapering and coating of NWs. Thus the 900 ^oC source temperature is ideal for GaAs NWs synthesis based on the NW density and morphology observed in SEM. But from the TEM observation (Figure 1f), most NWs are still heavily coated and these coatings need to be further minimized as they will hinder the NW device performance.

2.2. Reducing coatings by further tailoring V/III ratio

In order to reduce the surface coatings, the mechanism of coating formation has to be first understood. For this simple solid-source CVD technique, V/III ratio cannot be directly and independently controlled but can be instead tailored by adjusting the growth time and carrier gas flow together. When the growth prolongs, V/III ratio decreases gradually due to the persistent overpressure of As_2 vapor; therefore, less amount of As_2 would react with Ga in the catalyst/NW interface for the NW formation [6] and those excess Ga atoms would impinge onto and/or diffuse from the substrate to the NW surface as coatings and tapering via the vapor-solid (VS) mechanism [7]. In this regard, as shown in the Figure 2 (a), (b) and (c), the NW growth was shortened from 60 to 30 mins to aim for reduced surface coatings, without sacrificing the NW length.

On the other hand, as depicted in Figure 2 (a), (b) and (c), higher hydrogen flow or process pressure resulted in more surface coatings in the TEM inserts, due to the shorter mean free path and then more impingement of precursor

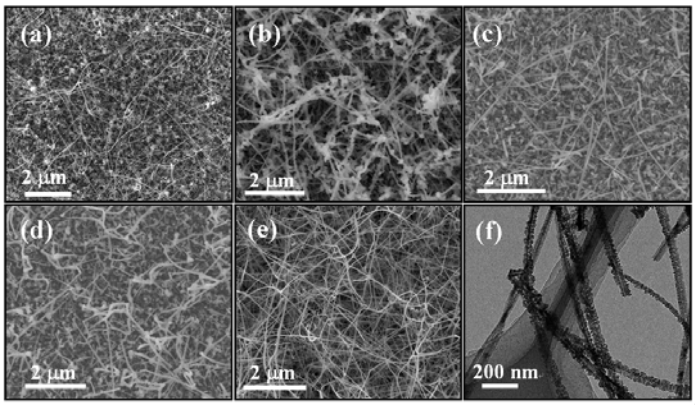

Figure 1. SEM images of GaAs NWs grown at source/substrate temperatures of: (a) 875/560 ^oC, (b) 875/600 ^oC, (c) 875/640 ^oC, (d) 850/600 ^oC and (e) 900/600 ^oC, and (f) is TEM image of (e). (H_2 flow rate of 200 sccm, ~0.95 torr, growth time of 60 min)

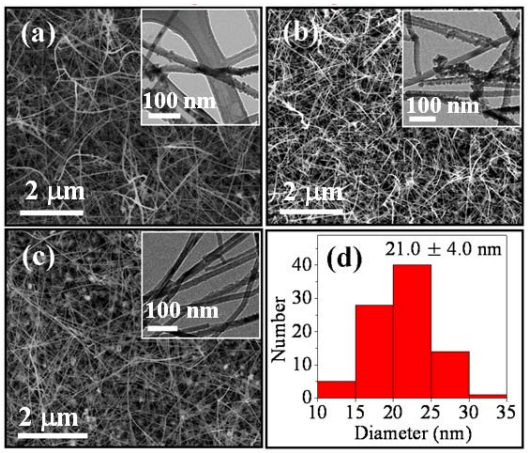

Figure 2. SEM and TEM (inset) images of GaAs NWs grown at H_2 flow of: (a) 200 sccm (~0.9 torr), (b) 400 sccm (~1.7 torr) and (c) 100 sccm (~0.4 torr), and (d) is diameter statistics of 98 NWs in TEM images of (c) inset. (Source/substrate temperatures are 900/600 ^{o}C, growth time is 30 min).

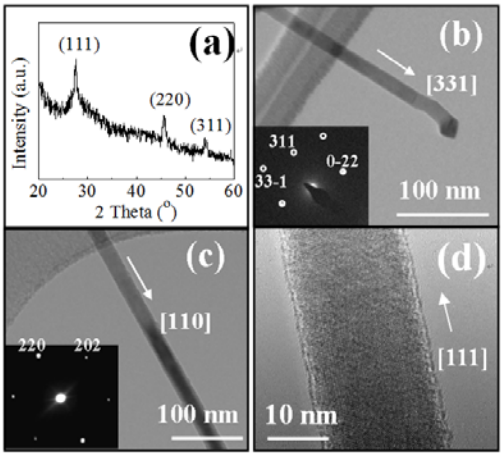

Figure 3. (a) is XRD pattern, (b) and (c) are TEM and SAED (zone axis of [-233] and [-111]) of GaAs NWs grown in [331] and [110] directions, and (d) is HRTEM image of NWs grown in <111> direction.

molecules onto the NW surface and substrates. In order to maintain the constant V/III ratio to reduce the coatings, a low hydrogen flow such as 100 sccm was utilized to maximize the retention time of precursors for the formation of uniform, long and relatively straight NWs (> 10 μm) with low defect density as demonstrated in Figure 2 (c) insert. Importantly, the NW diameters are uniform along the nanowire and no tapering is observed, confirming the optimal control of processing parameters in our growth. Notably, the NW diameters obtained from TEM is 21.0 ± 4.0 nm for a statistics of 98 NWs as shown in Figure 2 (d). This narrow diameter distribution is remarkably good considering the simplicity of this growth technique as compared to the sophisticated MBE and MOCVD system.

2.3. Chemical and structural characterization

The crystal quality and orientation of GaAs NWs grown at the optimal condition were studied by XRD and TEM as shown in Figure 3. The cubic zinc blende (ZB) structure (PDF 14-0450) is the dominant crystal phase with no peaks associated with hexagonal wurtzite (WZ) structure. The SAED patterns (Figure 3 (b)-(c)) also show the ZB structure of GaAs NWs which are consistent with the XRD results; however, there is a small proportion of NWs existed in the WZ phase (data not shown), probably due to the higher surface energy favorable in nanomaterials [8]. Importantly, there are no twin planes or defects observed, which could be attributed to the high supersaturation and good V/III ratio control during the growth. It is also noted that NWs are grown along different directions even though they are in the same ZB structure. Typically, NWs are grown along [111], [110] and [331] directions as depicted in Figure 3 (b)-(d), in which those low index planes are believed to have low surface energy and thus survives during the NW growth.

Moreover, the grown NWs have a 2-3 nm thick amorphous surface oxide layer as depicted in Figure 3 (d) and this layer thickness is consistent with the typical native oxide present on the surface of the bulk GaAs crystal. Based on the HRTEM image, the distances between the adjacent lattice planes are found to be 0.28 and 0.33 nm, which are in good agreement with the plane spacing of {200} and {111} families in the ZB structure. All these have suggested the grown NWs are highly crystalline with the low structural defect density.

3. Conclusions

In summary, crystalline GaAs NWs with a high growth yield are successfully synthesized by the solid-state CVD method on non-crystalline substrates, using Ni as catalysts. Notably, these NWs are grown with the low defect density and minimized surface coatings, in which these enhanced properties may have significant implications of GaAs NWs for various future technological applications.

4. Acknowledgements

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5. References

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