ORGANIC THIN FILM TRANSISTOR MEMORY BASED ON CDSE NANOPARTICLE/PMMA BLEND AS A TUNNELING LAYER

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Introduction

Organic thin-film transistors (OTFTs) have been studied with much interest over the last decade, due to their attractive features such as low cost, low temperature processing and mechanical flexibility [1-3]. Recently, much attention is paid to organic memory devices. Nanoparticles (NPs) based device is a promising candidate for the future nonvolatile memory. Because it is advantageous in terms of low power consumption, small device size, excellent stress leakage current induced (SILC) immunity and better retention [4,5]. For these reasons, we have fabricated non-volatile pentacene TFTs memory with CdSe NPs on the gate insulator. As an organic insulator, polymethylmethacrylate (PMMA) has been investigated because of its high resistivity, no hysteresis, thermal stability, and easy fabrication at low temperature. In this study, we realized the NPs floating gate memory with CdSe NPs dispersed in PMMA insulating layer. The unique feature of this study is that the multi-layers of CdSe NPs are formed inside the PMMA tunneling insulator, which provides a large memory window, potential multilevel charging characteristics, and improved retention properties.

Experimental

The metal-insulator-semiconductor (MIS) structure and top-contact pentacene thin film transistors (TFTs) were fabricated on the indium tin oxide (ITO) glass substrate. The ITO layer was used as gate electrode. As a control device without CdSe NPs, PMMA (molecular weight 950K, diluted in 4% anisole) as a gate insulator, was spin-coated twice at 4500 rpm for 60 seconds over ITO and subsequently baked at 160 ^{o}C for 30 min in a conventional oven. In this way, the thickness of PMMA layer was about 400 nm. For the NPs floating gate memory, the CdSe NPs solution (30 wt%) was mixed with PMMA solution. The CdSe NPs/PMMA layer was spin-coated on PMMA layer (200 nm) and subsequently baked at 160 ^{o}C for 30 min in a conventional oven to make PMMA gate insulator having homogeneously distributed CdSe NPs inside PMMA. The CdSe NPs were dispersed in hexane with a concentration of an order of 10^{16} /ml. The pentacene layer was deposited by thermal evaporation at a rate of 0.1 Å/s to a thickness of about 70 nm at a high vacuum of less than 5×10^{-6} torr. In MIS structure, a top metal electrode of Au was subsequently deposited by thermal evaporation through a shadow mask of 500 μm diameter size. In pentacene TFTs, the source and drain electrodes, a 100 nm thick Au layer were deposited through the shadow mask by thermal evaporation. The pentacene TFTs obtained thereby had a channel length (L) and width (W) of 100 μm and 1000 μm respectively (Fig. 1). The electrical properties of devices were analyzed by capacitance-voltage (C-V) and current-voltage (I-V) characteristics at room temperature in ambient air using Agilent 4284A and Keithley 236 meter at a frequency of 100 kHz.

Result and Discussion

We have observed the charging/discharging effect of CdSe NPs, using C-V and I-V measurement. The flatband voltage shift (ΔV_{FB}) was not observed in a control device without CdSe NPs when a gate voltage was swept. On the other hand, a hysteresis loops in counterclockwise direction were clearly observed in the memory device with CdSe NPs when the V_{GS} was swept from +10 to -10 V, and then back to +10 V. Then, the sweeping V_{GS} was increased up to +/-30 V (Fig. 2). Compared to the hysteresis in the range of +/-30 V, the C-V curve shifted to negative direction, which means

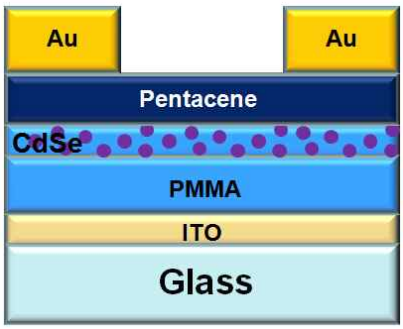

Fig 1. Schematic of the CdSe NPs/PMMA composition in the blend as the tunneling layer for non-volatile organic memory.

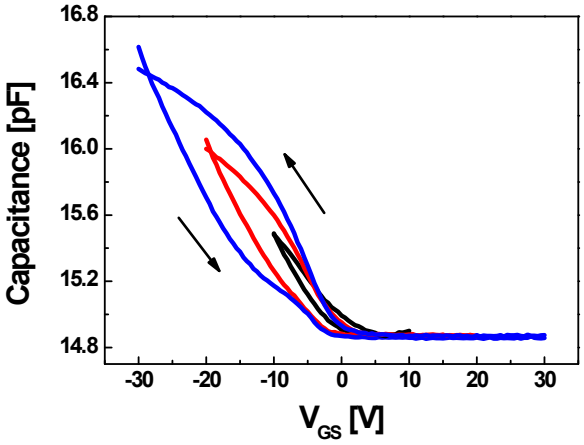

Fig 2. The C-V characteristic of the fabricated organic memory at different V_{GS} sweeping range.

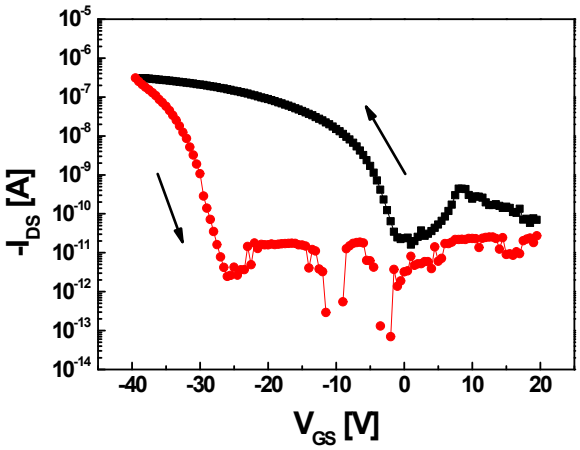

Fig 3. The I-V characteristic of the fabricated organic memory at different V_{GS} sweeping range.

that CdSe NPs are positively charged, when the negative V_{GS} is applied. The negative shift during application of negative V_{GS} indicates that holes are transported from a pentacene layer to CdSe NPs or electrons are withdrawn from CdSe NPs. The shift of C-V curve, representing memory window, increased as increasing the V_{GS} sweep, by the increased charge injection. It should be noted that no shift was observed when the V_{GS} was swept from positive to negative direction. It means that the positive charging of CdSe NPs can be achieved more efficiently than its negative charging on this device.

Also, in I-V analysis, a hysteresis loop in counterclockwise direction was clearly observed in the memory device with CdSe NPs when the V_{GS} was swept from +20 to -40 V, and then back to +20 V (Fig. 3).

Conclusion

We demonstrated a CdSe NPs/polymer blend as the tunneling layer for non-volatile organic memory. The charging and discharging CdSe NPs were observed in the C-V, I-V analysis, showing the sufficiently large memory window. This approach, by virtue of its simplicity in processing, can realize integrated organic memory devices in low-cost plastic electronics applications.

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