PREPARATION OF DIELECTRIC EMBEDDED SILICON NANOCRYSTALLITES FOR FLASH MEMORY APPLICATIONS

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Dielectric embedded silicon nanocrystallites (SiNCs) have several unique features which have led to several novel applications. The embedded SiNCs can produce strong light emission because of quantum confinement effects. The excellent dielectric passivation made the light emitting from dielectric embedded SiNCs be stable and high efficient [1]. A novel structure for a silicon-based light emitting device has been proposed [2]. The dielectric embedded SiNCs were also found to be an excellent candidate for memory devices. The SiNCs or excess silicon in silicon oxide or nitride are both electron and hole deep traps. The localized electron or hole in these traps can last for over 10 years at room temperature. This excellent property well suits for flash memory applications [3]. Fig.1 illustrates the schematic view of this kind structure where the conventional single polysilicon floating gate is replaced with a number of well-isolated nano-particles for the charge storage. This structure will reduce the possibility of charge loss encountered in the conventional floating gate structure. It demonstrated several improvements on the programming speed, charge retention capability, and operation voltage [4].

In this work, the silicon nitride films with SiNC embedment were grown by a CMOS compatible process. A silicon-rich silicon nitride films was first grown by low-pressure chemical vapor deposition technique and then a high-temperature annealing was conducted. In present experiment, SiNCs with sizes of 1 to 4 nm (in diameter) were formed as a result of phase separation effect (see Fig.2). We use silicon nitride because it has low barriers at the Si-Si_3N_4 interface for hole (2.0 eV) and electron (1.5 eV) injection and a low field (2-4 MV/cm) carrier injection is possible. X-ray photoelectron spectroscopy (XPS) analyses on chemical bonding structures indicate that the as-deposited Si-rich film can be described by a random bonding model [5]. In the as-deposited sample, the bonding energy of Si 2p is in the range of 100 to 104 eV (see Fig.3). After annealing in oxygen ambient at 950 ^{o}C for 30 min, phase separation effect is observed. The crystalline Si phase (99.5 eV) and silicon nitride phase (~101 eV) are more obvious. Fig.4 depicts the capacitance-voltage curves of both as-deposited and annealing samples. Large hysteresis is observed for both samples indicating significant charge trapping. However, the charge trapping mechanisms are different. In the as deposited sample, the charge trapping is due to the Si-Si defects whereas in annealed sample the charges are localized in SiNCs and results in a larger hysteresis. The current-voltage characteristics in Fig.5 indicate that the as-deposited sample has very poor insulating properties because the high amount of dielectric defects give rise to significant trap-assisted tunneling. After high-temperature annealing, the breakdown voltage is increased to over 8 V. These observations indicate that the current conduction and charge localization mechanism in as-deposited and annealed samples are different. The annealed sample has better insulating properties and it improves the blocking capability and then the retention time. Moreover, since the charges are localized in the SiNCs, it is more robust again erroneous erase and has large memory window.

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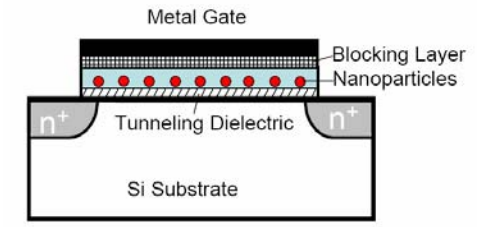

Fig.1. Structure of flash memory cell based on silicon nitride embedded silicon nanoparticles.

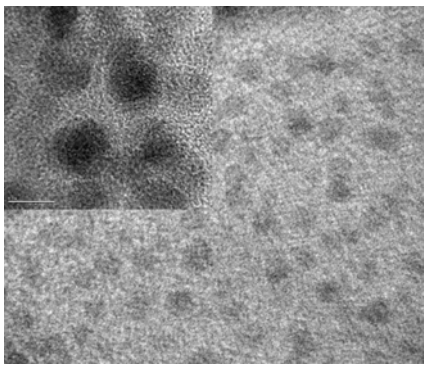

Fig.2. TEM micrograph showing the silicon nanoparticles embedded in a silicon nitride film.

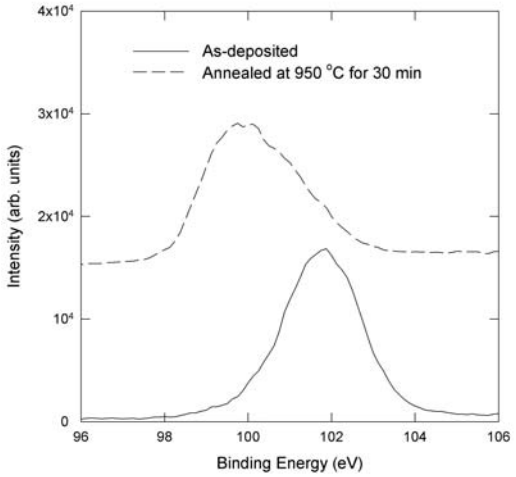

Fig.3. Si 2p XPS spectra for as-deposited and high-temperature annealed silicon nitride films.

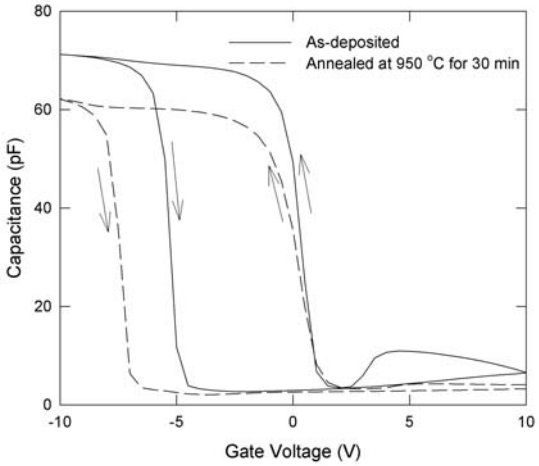

Fig.4. C-V characteristics of MOS capacitors showing the hysteresis due to charge localization in dielectric traps or embedded silicon nanoparticles.

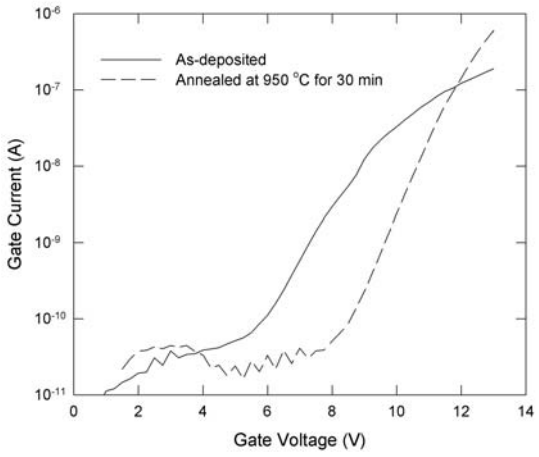

Fig.5. Current-voltage characteristics of MOS capacitors with different gate dielectric films.